09/281,973

claim 1 use fig. 1 prior art to reject

6,148,099

```
     FILE 'USPATFULL' ENTERED AT 16:52:38 ON 23 JAN 2001
L1          5952 S TEST CIRCUIT#
L2           154 S MIROCONTROLLER UNIT OR MICROCONTROLLER DEVICE
L3            49 S  1 (P) L2
L4          5981 S FIRST PIN#
L5         40087 S FIRST SIGNAL#
L6            23 S L4 (P) L5
L7          7856 S SECOND PIN#
L8         43028 S SECOND SIGNAL#
L9            23 S L7 (P) L8
L10           15 S L9 (P) L6
L11           63 S TEST SIGNAL GENERATING CIRCUIT#
L12           63 S TEST SIGNAL GENERATING CIRCUIT#
L13        10211 S TEST SIGNAL#
L14           63 S L12 (P) L13
L15        40891 S LOGIC CIRCUIT
L16       307243 S COUNTER#
L17         6729 S L15 (P) L16
L18        67200 S CLOCK SIGNAL#
L19        28430 S RESET SIGNAL#
L20            2 S L10 AND L18
L21            1 S L10 AND L19
                 SAVE TESTCIRCUIT/L ALL
L22       116180 S HIGH LEVEL
L23         7137 S TEST MODE
L24          184 S CLOCK PIN (P) CLOCK SIGNAL#
L25          262 S RESET PIN (P) RESET SIGNAL#
L26            2 S L3 (P) L23
L27            1 S L26 AND L25
L28          437 S (L18 OR L19) AND (L24 OR L25)
L29          309 S L28 AND (L15 OR L16)
L30          154 S L29 AND (L22 OR L23)
L31            2 S L20 AND (L4 OR L5)
                 SAVE TESTCIRCUIT/L ALL

=> d l31 ibib ti 1-2


L31  ANSWER 1 OF (2) USPATFULL
ACCESSION NUMBER:         2000:154899  USPATFULL
TITLE:                    System for and method of connecting a hardware
modeling
                          element to a hardware modeling system
INVENTOR(S):              Papamarcos, Mark Stanley, San Jose, CA, United States
                          Read, Andrew Jefferson, Sunnyvale, CA, United States
                          Heideman, Wayne Phillip, San Jose, CA, United States
                          Mardjuki, Robert Kristianto, Peasanton, CA, United
                          States
                          Couch, Robert Kimberly, Santa Cruz, CA, United States
                          Jaeger, Peter Ralph, San Jose, CA, United States
                          Kappauf, William Fitch, San Jose, CA, United States
                          Rudin, Melvin, Los Altso, CA, United States
                          Kelly, Norman Francis, San Jose, CA, United States
                          Widdoes, Jr., Lawrence Curtis, Los Altos Hill, CA,
                          United States
PATENT ASSIGNEE(S):       Synopsys, Inc., Mountain View, CA, United States (U.S.
                          corporation)
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	NUMBER	DATE	
PATENT INFORMATION:	US 6148275	20001114	
APPLICATION INFO.:	US 1997-919635	19970828	(8)

RELATED APPLN. INFO.: Continuation of Ser. No. US 1994-312198, filed on 26 Sep 1994 which is a continuation of Ser. No. US 1991-780529, filed on 18 Oct 1991, now patented, Pat. No. US 5369593 which is a continuation of Ser. No. US 1989-359624, filed on 31 May 1989, now abandoned

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Teska, Kevin J.
ASSISTANT EXAMINER: Jones, Hugh
LEGAL REPRESENTATIVE: Haverstock & Owens LLP
NUMBER OF CLAIMS: 69
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 24 Drawing Figure(s); 8 Drawing Page(s)
LINE COUNT: 1368
TI System for and method of connecting a hardware modeling element to a hardware modeling system

L31 ANSWER 2 OF 2 USPATFULL
ACCESSION NUMBER: 79:17116 USPATFULL
TITLE: Memory device having a minimum number of pins
INVENTOR(S): Lauffer, Donald K., Poway, CA, United States
Ward, William P., Poway, CA, United States
PATENT ASSIGNEE(S): NCR Corporation, Dayton, OH, United States (U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 4148099	19790403	
APPLICATION INFO.:	US 1978-895329	19780411	(5)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Fears, Terrell W.
LEGAL REPRESENTATIVE: Cavender, J. T.; Dugas, Edward; Jewett, Stephen F.
NUMBER OF CLAIMS: 16
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 5 Drawing Figure(s); 3 Drawing Page(s)
LINE COUNT: 458
TI Memory device having a minimum number of pins

=> d l27 ibib ti

L27 ANSWER 1 OF 1 USPATFULL
ACCESSION NUMBER: 1999:153005 USPATFULL
TITLE: Microcontroller having special mode enable detection circuitry and a method of operation therefore
INVENTOR(S): Hull, Richard L., Chandler, AZ, United States
Ellison, Scott, Chandler, AZ, United States
Hofhine, Paul, Mesa, AZ, United States
PATENT ASSIGNEE(S): Microchip Technology Incorporated, Chandler, AZ, United States (U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 5991910	19991123	
APPLICATION INFO.:	US 1997-960636	19971029	(8)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Auve, Glenn A.
LEGAL REPRESENTATIVE: Katz, Paul N.; Chichester, Ronald L.Frohwitter
NUMBER OF CLAIMS: 19
EXEMPLARY CLAIM: 10

NUMBER OF DRAWINGS: 4 Drawing Figure(s); 2 Drawing Page(s)
LINE COUNT: 552
TI Microcontroller having special mode enable detection circuitry and a method of operation therefore

=> d l26 ibib ti 1-2

L26 ANSWER 1 OF 2 USPATFULL
ACCESSION NUMBER: 1999:153005 USPATFULL
TITLE: Microcontroller having special mode enable detection circuitry and a method of operation therefore
INVENTOR(S): Hull, Richard L., Chandler, AZ, United States
Ellison, Scott, Chandler, AZ, United States
Hofhine, Paul, Mesa, AZ, United States
PATENT ASSIGNEE(S): Microchip Technology Incorporated, Chandler, AZ, United States (U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 5991910	19991123	
APPLICATION INFO.:	US 1997-960636	19971029	(8)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Auve, Glenn A.
LEGAL REPRESENTATIVE: Katz, Paul N.; Chichester, Ronald L.Frohwitter
NUMBER OF CLAIMS: 19
EXEMPLARY CLAIM: 10
NUMBER OF DRAWINGS: 4 Drawing Figure(s); 2 Drawing Page(s)
LINE COUNT: 552
TI Microcontroller having special mode enable detection circuitry and a method of operation therefore

L26 ANSWER 2 OF 2 USPATFULL
ACCESSION NUMBER: 89:51847 USPATFULL
TITLE: Architecture modification for improved ROM security
INVENTOR(S): Ong, Dewitt, Tempe, AZ, United States
Rider, Scott, Chandler, AZ, United States
PATENT ASSIGNEE(S): Intel Corporation, Santa Clara, CA, United States (U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 4843026	19890627	
APPLICATION INFO.:	US 1987-101206	19870924	(7)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Hearn, Brian E.
ASSISTANT EXAMINER: Thomas, Tom
LEGAL REPRESENTATIVE: Blakely, Sokoloff, Taylor & Zafman
NUMBER OF CLAIMS: 4
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 8 Drawing Figure(s); 3 Drawing Page(s)
LINE COUNT: 380
TI Architecture modification for improved ROM security

=> d l21 ibib ti

L21 ANSWER 1 OF 1 USPATFULL
ACCESSION NUMBER: 1998:63062 USPATFULL
TITLE: Method and apparatus for logic network interfacing with

automatic receiver node and transmit node selection capability

INVENTOR(S): Allen, Charles M., Sunnyvale, CA, United States
PATENT ASSIGNEE(S): Maxim Integrated Products, Sunnyvale, CA, United States

(U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 5761463	19980602
APPLICATION INFO.:	US 1997-808193	19970228 (8)

RELATED APPLN. INFO.: Continuation of Ser. No. US 1994-365355, filed on 28 Dec 1994, now abandoned

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Harvey, Jack B.
ASSISTANT EXAMINER: Etienne, Ario
LEGAL REPRESENTATIVE: Blakely, Sokoloff, Taylor & Zafman LLP
NUMBER OF CLAIMS: 44
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 5 Drawing Figure(s); 4 Drawing Page(s)
LINE COUNT: 764
TI Method and apparatus for logic network interfacing with automatic receiver node and transmit node selection capability

=> d l20 ibib ti 1-2

L20 ANSWER 1 OF 2 USPATFULL
ACCESSION NUMBER: 2000:154899 USPATFULL
TITLE: System for and method of connecting a hardware modeling element to a hardware modeling system

INVENTOR(S): Papamarcos, Mark Stanley, San Jose, CA, United States
Read, Andrew Jefferson, Sunnyvale, CA, United States
Heideman, Wayne Phillip, San Jose, CA, United States
Mardjuki, Robert Kristianto, Peasanton, CA, United States
Couch, Robert Kimberly, Santa Cruz, CA, United States
Jaeger, Peter Ralph, San Jose, CA, United States
Kappauf, William Fitch, San Jose, CA, United States
Rudin, Melvin, Los Altso, CA, United States
Kelly, Norman Francis, San Jose, CA, United States
Widdoes, Jr., Lawrence Curtis, Los Altos Hill, CA, United States
PATENT ASSIGNEE(S): Synopsys, Inc., Mountain View, CA, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 6148275	20001114
APPLICATION INFO.:	US 1997-919635	19970828 (8)

RELATED APPLN. INFO.: Continuation of Ser. No. US 1994-312198, filed on 26 Sep 1994 which is a continuation of Ser. No. US 1991-780529, filed on 18 Oct 1991, now patented, Pat. No. US 5369593 which is a continuation of Ser. No. US 1989-359624, filed on 31 May 1989, now abandoned

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Teska, Kevin J.
ASSISTANT EXAMINER: Jones, Hugh
LEGAL REPRESENTATIVE: Haverstock & Owens LLP
NUMBER OF CLAIMS: 69
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 24 Drawing Figure(s); 8 Drawing Page(s)
LINE COUNT: 1368

TI System for and method of connecting a hardware modeling element to a hardware modeling system

L20 ANSWER 2 OF 2 USPATFULL

ACCESSION NUMBER:	79:17116 USPATFULL
TITLE:	Memory device having a minimum number of pins
INVENTOR(S):	Lauffer, Donald K., Poway, CA, United States Ward, William P., Poway, CA, United States
PATENT ASSIGNEE(S):	NCR Corporation, Dayton, OH, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4148099	19790403
APPLICATION INFO.:	US 1978-895329	19780411 (5)

DOCUMENT TYPE:	Utility
PRIMARY EXAMINER:	Fears, Terrell W.
LEGAL REPRESENTATIVE:	Cavender, J. T.; Dugas, Edward; Jewett, Stephen F.
NUMBER OF CLAIMS:	16
EXEMPLARY CLAIM:	1
NUMBER OF DRAWINGS:	5 Drawing Figure(s); 3 Drawing Page(s)
LINE COUNT:	458

TI Memory device having a minimum number of pins

=> d l10 ibib ti 1-15

L10 ANSWER 1 OF 15 USPATFULL

ACCESSION NUMBER:	2000:154899 USPATFULL
TITLE:	System for and method of connecting a hardware modeling element to a hardware modeling system
INVENTOR(S):	Papamarcos, Mark Stanley, San Jose, CA, United States Read, Andrew Jefferson, Sunnyvale, CA, United States Heideman, Wayne Phillip, San Jose, CA, United States Mardjuki, Robert Kristianto, Peasanton, CA, United States Couch, Robert Kimberly, Santa Cruz, CA, United States Jaeger, Peter Ralph, San Jose, CA, United States Kappauf, William Fitch, San Jose, CA, United States Rudin, Melvin, Los Altso, CA, United States Kelly, Norman Francis, San Jose, CA, United States Widdoes, Jr., Lawrence Curtis, Los Altos Hill, CA, United States
PATENT ASSIGNEE(S):	Synopsys, Inc., Mountain View, CA, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 6148275	20001114
APPLICATION INFO.:	US 1997-919635	19970828 (8)

RELATED APPLN. INFO.:	Continuation of Ser. No. US 1994-312198, filed on 26 Sep 1994 which is a continuation of Ser. No. US 1991-780529, filed on 18 Oct 1991, now patented, Pat. No. US 5369593 which is a continuation of Ser. No. US 1989-359624, filed on 31 May 1989, now abandoned
DOCUMENT TYPE:	Utility
PRIMARY EXAMINER:	Teska, Kevin J.
ASSISTANT EXAMINER:	Jones, Hugh
LEGAL REPRESENTATIVE:	Haverstock & Owens LLP
NUMBER OF CLAIMS:	69
EXEMPLARY CLAIM:	1
NUMBER OF DRAWINGS:	24 Drawing Figure(s); 8 Drawing Page(s)
LINE COUNT:	1368

TI System for and method of connecting a hardware modeling element to a hardware modeling system

L10 ANSWER 2 OF 15 USPATFULL
ACCESSION NUMBER: 2000:62058 USPATFULL
TITLE: I/O pin electronics circuit having a pair of drivers
INVENTOR(S): Yoshiba, Kazumichi, Gyoda, Japan
PATENT ASSIGNEE(S): Advantest Corp., Tokyo, Japan (non-U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 6064242	20000516	
	WO 9724622	19971007	
APPLICATION INFO.:	US 1997-817755	19970623	(8)
	WO 1995-JP2744	19951228	
		19970623	PCT 371 date
		19970623	PCT 102(e) date

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Wells, Kenneth B.
ASSISTANT EXAMINER: Nguyen, Minh
LEGAL REPRESENTATIVE: Muramatsu & Associates
NUMBER OF CLAIMS: 9
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 11 Drawing Figure(s); 8 Drawing Page(s)
LINE COUNT: 282
TI I/O pin electronics circuit having a pair of drivers

L10 ANSWER 3 OF 15 USPATFULL
ACCESSION NUMBER: 1999:133812 USPATFULL
TITLE: Interconnection arrangement for distribution of electrical signal
INVENTOR(S): Meyer, Charles S., Nevada City, CA, United States
PATENT ASSIGNEE(S): NVision, Inc., Grass Valley, CA, United States (U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 5973933	19991026	
APPLICATION INFO.:	US 1998-74637	19980507	(9)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Abrams, Neil
ASSISTANT EXAMINER: Duverne, J. F.
LEGAL REPRESENTATIVE: Smith-Hill and Bedell
NUMBER OF CLAIMS: 12
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 9 Drawing Figure(s); 5 Drawing Page(s)
LINE COUNT: 599
TI Interconnection arrangement for distribution of electrical signal

L10 ANSWER 4 OF 15 USPATFULL
ACCESSION NUMBER: 1999:107496 USPATFULL
TITLE: Two connector SIMM format interface circuit
INVENTOR(S): Donovan, Hans, Mount Airy, MD, United States
Hicks, Thomas R., Cranberry Twp, PA, United States
PATENT ASSIGNEE(S): Hughes Electronics Corporation, El Segundo, CA, United States (U.S. corporation)

	NUMBER	DATE	
PATENT INFORMATION:	US 5949824	19990907	
APPLICATION INFO.:	US 1996-604121	19960220	(8)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Bocure, Tesfaldet
LEGAL REPRESENTATIVE: Whelan, John T.; Sales, Michael W.
NUMBER OF CLAIMS: 3

EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 3 Drawing Figure(s); 2 Draw Page(s)
LINE COUNT: 262
TI Two connector SIMM format interface circuit

L10 ANSWER 5 OF 15 USPATFULL
ACCESSION NUMBER: 1998:63062 USPATFULL
TITLE: Method and apparatus for logic network interfacing with
automatic receiver node and transmit node selection capability
INVENTOR(S): Allen, Charles M., Sunnyvale, CA, United States
PATENT ASSIGNEE(S): Maxim Integrated Products, Sunnyvale, CA, United States
(U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 5761463	19980602
APPLICATION INFO.:	US 1997-808193	19970228 (8)

RELATED APPLN. INFO.: Continuation of Ser. No. US 1994-365355, filed on 28 Dec 1994, now abandoned
DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Harvey, Jack B.
ASSISTANT EXAMINER: Etienne, Ario
LEGAL REPRESENTATIVE: Blakely, Sokoloff, Taylor & Zafman LLP
NUMBER OF CLAIMS: 44
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 5 Drawing Figure(s); 4 Drawing Page(s)
LINE COUNT: 764
TI Method and apparatus for logic network interfacing with automatic receiver node and transmit node selection capability

L10 ANSWER 6 OF 15 USPATFULL
ACCESSION NUMBER: 96:102214 USPATFULL
TITLE: Distributed NOR tag match apparatus
INVENTOR(S): McClure, David C., Carrollton, TX, United States
PATENT ASSIGNEE(S): SGS-Thomson Microelectronics, Inc., Carrollton, TX, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 5572456	19961105
APPLICATION INFO.:	US 1993-114747	19930831 (8)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Dinh, Son T.
LEGAL REPRESENTATIVE: Galanthay, Theodore E.; Hill, Kenneth C.; Jorgenson, Lisa K.
NUMBER OF CLAIMS: 23
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 9 Drawing Figure(s); 3 Drawing Page(s)
LINE COUNT: 490
TI Distributed NOR tag match apparatus

L10 ANSWER 7 OF 15 USPATFULL
ACCESSION NUMBER: 91:65262 USPATFULL
TITLE: Personal computer based non-interactive monitoring of communication links
INVENTOR(S): Al-Salameth, Daniel Y., Marlboro, NJ, United States
Farah, Jeffrey J., Newark, NJ, United States
Soukas, John, Freehold, NJ, United States
PATENT ASSIGNEE(S): AT&T Bell Laboratories, Murray Hill, NJ, United States (U.S. corporation)

	NUMBER	DATE

	NUMBER	DATE
PATENT INFORMATION:	US 5040111	19910813
APPLICATION INFO.:	US 1988-179692	19880411 (7)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Shaw, Gareth D.
ASSISTANT EXAMINER: Wayher, Paul
LEGAL REPRESENTATIVE: Weiss, Eli
NUMBER OF CLAIMS: 1
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 8 Drawing Figure(s); 7 Drawing Page(s)
LINE COUNT: 304
TI Personal computer based non-interactive monitoring of communication links

L10 ANSWER 8 OF 15 USPATFULL
ACCESSION NUMBER: 88:8627 USPATFULL
TITLE: Transmit/receive module for phased array antenna system
INVENTOR(S): Fithian, Michael J., Boulder, CO, United States
Hirsch, Vincent A., Boulder, CO, United States
Zurawski, Kenneth R., Lafayette, CO, United States
Medina, Alvaro, Boulder, CO, United States
PATENT ASSIGNEE(S): Ball Corporation, Muncie, IN, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4724441	19880209
APPLICATION INFO.:	US 1986-867848	19860523 (6)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Blum, Theodore M.
ASSISTANT EXAMINER: Gregory, Bernarr E.
LEGAL REPRESENTATIVE: Alberding, Gilbert E.
NUMBER OF CLAIMS: 11
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 4 Drawing Figure(s); 2 Drawing Page(s)
LINE COUNT: 431
TI Transmit/receive module for phased array antenna system

L10 ANSWER 9 OF 15 USPATFULL
ACCESSION NUMBER: 87:59020 USPATFULL
TITLE: Device for opening and closing a shutter member of a disk cartridge
INVENTOR(S): Nakagawa, Kenzo, Kanagawa, Japan
Suzuki, Masayuki, Tokyo, Japan
PATENT ASSIGNEE(S): Sony Corporation, Tokyo, Japan (non-U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4688206	19870818
APPLICATION INFO.:	US 1986-905491	19860910 (6)

	NUMBER	DATE
PRIORITY INFORMATION:	JP 1985-209537	19850923

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Stephan, Steven L.
LEGAL REPRESENTATIVE: Eslinger, Lewis H.; Sinderbrand, Alvin
NUMBER OF CLAIMS: 4
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 10 Drawing Figure(s); 8 Drawing Page(s)
LINE COUNT: 614
TI Device for opening and closing a shutter member of a disk cartridge

L10 ANSWER 10 OF 15 USPATFULL

ACCESSION NUMBER: 87:13587 USPATFULL
TITLE: Signal attenuation circuit
INVENTOR(S): Brown, Mark J., Phoenix, AZ, United States
PATENT ASSIGNEE(S): Motorola, Inc., Schaumburg, IL, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4646036	19870224
APPLICATION INFO.:	US 1985-812883	19851223 (6)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Mullins, James B.
LEGAL REPRESENTATIVE: Gresham, Lowell W.
NUMBER OF CLAIMS: 10
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 3 Drawing Figure(s); 2 Drawing Page(s)
LINE COUNT: 441
TI Signal attenuation circuit

L10 ANSWER 11 OF 15 USPATFULL
ACCESSION NUMBER: 87:12773 USPATFULL
TITLE: Apparatus and method for monitoring the readiness for operation of a power chuck
INVENTOR(S): Hiestand, Karl, Pfullendorf, Germany, Federal Republic of
PATENT ASSIGNEE(S): SMW Schneider & Weisshaupt GmbH, Germany, Federal Republic of (non-U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4645220	19870224
APPLICATION INFO.:	US 1985-695445	19850128 (6)

	NUMBER	DATE
PRIORITY INFORMATION:	DE 1984-3402988	19840128

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Weidenfeld, Gil
ASSISTANT EXAMINER: Howell, Daniel W.
LEGAL REPRESENTATIVE: McGlew and Tuttle
NUMBER OF CLAIMS: 6
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 1 Drawing Figure(s); 1 Drawing Page(s)
LINE COUNT: 273
TI Apparatus and method for monitoring the readiness for operation of a power chuck

L10 ANSWER 12 OF 15 USPATFULL
ACCESSION NUMBER: 79:17116 USPATFULL
TITLE: Memory device having a minimum number of pins
INVENTOR(S): Lauffer, Donald K., Poway, CA, United States
Ward, William P., Poway, CA, United States
PATENT ASSIGNEE(S): NCR Corporation, Dayton, OH, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4148099	19790403
APPLICATION INFO.:	US 1978-895329	19780411 (5)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Fears, Terrell W.
LEGAL REPRESENTATIVE: Cavender, J. T.; Dugas, Edward; Jewett, Stephen F.
NUMBER OF CLAIMS: 16
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 5 Drawing Figure(s); 3 Drawing Page(s)

LINE COUNT: 458
TI Memory devi[redacted]having a minimum number of pin[redacted]

L10 ANSWER 13 OF 15 USPATFULL
ACCESSION NUMBER: 79:14642 USPATFULL
TITLE: Memory device having a reduced number of pins
INVENTOR(S): Ward, William P., Poway, CA, United States
Lauffer, Donald K., Poway, CA, United States
PATENT ASSIGNEE(S): NCR Corporation, Dayton, OH, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 4145760	19790320
APPLICATION INFO.:	US 1978-895328	19780411 (5)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Fears, Terrell W.
LEGAL REPRESENTATIVE: Cavender, J. T.; Dugas, Edward; Jewett, Stephen F.
NUMBER OF CLAIMS: 12
EXEMPLARY CLAIM: 10
NUMBER OF DRAWINGS: 5 Drawing Figure(s); 3 Drawing Page(s)
LINE COUNT: 434
TI Memory device having a reduced number of pins

L10 ANSWER 14 OF 15 USPATFULL
ACCESSION NUMBER: 79:4903 USPATFULL
TITLE: Error compensator for a timepiece
INVENTOR(S): Leonard, Vivian A., 1200 Cordell St., Denton, TX, United States 76201

	NUMBER	DATE
PATENT INFORMATION:	US 4136513	19790130
APPLICATION INFO.:	US 1976-733299	19761018 (5)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Jackmon, Edith S.
LEGAL REPRESENTATIVE: Richards, Harris & Medlock
NUMBER OF CLAIMS: 10
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 6 Drawing Figure(s); 1 Drawing Page(s)
LINE COUNT: 371
TI Error compensator for a timepiece

L10 ANSWER 15 OF 15 USPATFULL
ACCESSION NUMBER: 75:38144 USPATFULL
TITLE: Reverberation condition adaptive sonar receiving system
and method
INVENTOR(S): Mackey, Larry C., Greensburg, PA, United States
Kozlowski, Dennis C., Lutherville, MD, United States
PATENT ASSIGNEE(S): Westinghouse Electric Corporation, Pittsburgh, PA, United States (U.S. corporation)

	NUMBER	DATE
PATENT INFORMATION:	US 3896411	19750722
APPLICATION INFO.:	US 1974-443874	19740219 (5)

DOCUMENT TYPE: Utility
PRIMARY EXAMINER: Farley, Richard A.
LEGAL REPRESENTATIVE: Schron, D.
NUMBER OF CLAIMS: 11
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 8 Drawing Figure(s); 5 Drawing Page(s)
LINE COUNT: 751
TI Reverberation condition adaptive sonar receiving system and method

> d l31 kwic 1-2

L31 ANSWER 1 OF 2 USPATFULL

SUMM . . . damaged. The DAB preferably includes a keepalive clocking circuit that connects to the clock pins of the HME to provide **clock signals** to the HME circuitry. The keepalive circuitry keeps the HME refreshed when it is not being accessed by the HMS.

DETD TABLE 1

Signals	Direction	Description
CLK10MHZ	From PEL to DAB	The two keep-alive **clock signals**.
CLK1MHZ		
EECLK	From PEL to DAB	The clock to the DAB EEPROM
EEIN	From PEL to DAB	The serial input to the DAB. . .

DETD . . . shows keepalive clock circuitry 154 of FIG. 1. Referring to FIGS. 1 and 22, system connector 102 receives two keepalive **clock signals** and an enable signal from the PEL. The system connector provides these signals to the keepalive clock circuitry via parallel. . .

CLM What is claimed is:

. . . 1 wherein the generation circuit further comprises a voltage regulator coupled to the one or more segments for receiving a **first signal** from the hardware modeling system for forming a second signal and a switch for selecting one of the **first signal** and the second signal for powering the electronic device.

19. The system as claimed in claim 18 wherein the connector comprises first, second and third segments, wherein the first segment includes a **first pin** longer than a second pin within the second segment and longer than a third pin within the third segment, wherein. . .

. . . 24 wherein the generation circuit further comprises a voltage regulator coupled to the one or more segments for receiving a **first signal** from the hardware modeling system for forming a second signal and a switch for selecting one of the **first signal** and the second signal for powering the hardware modeling element.

27. A hardware modeling system for simulating a circuit and providing signals to and measuring responses from a hardware modeling. . . modeling system is powered including: i. electrostatic charge dissipation circuitry to dissipate electrostatic charge; ii. a first segment including a **first pin** of a first length coupled to the electrostatic charge dissipation circuitry; iii. ground equalization circuitry to equalize ground levels of the connector, the hardware modeling system and the hardware modeling element; iv. a second segment including a **second pin** of a second length coupled to the ground equalization circuitry; v. power supply control circuitry to supply power from the. . . length is longer than the third length such that when the connector is inserted into the hardware modeling system, the **first pin** engages the hardware

modeling system first, the **second pin** engages the hardware modeling system second and the third pin engages the hardware modeling system third; b. a grid adapter. . . . and providing electrical signals to the hardware modeling element including a voltage regulator coupled to the connector for receiving a **first signal** and forming a **second signal**, and a switch for selecting between a selective one of the **first signal** and the **second signal** for powering the hardware modeling element; and d. a memory circuit for storing and providing information to the hardware modeling. . . . . wherein the one or more segments include first, second, and third segments wherein the first segment comprises at least one **first pin** that is longer than pins within the second and third segments and wherein the second segment comprises at least one. . . . . generation circuit further comprises: (2) a voltage regulator coupled to the one or more segments and configured for receiving a **first signal** from the hardware modeling system, and forming a second signal; and (3) a switch coupled to receive the **first signal** and the second signal and configured for selecting one of the **first signal** and the second signal for powering the selected electronic device.

L31 ANSWER 2 OF 2 USPATFULL

AB . . . internal power supply. At other times during the receipt of signals on the two external pins, the signal on the **first pin** provides both memory select and clocking functions and the signal on the second pin provides memory mode select, address, and. . .

DETD . . . lines 70 to provide the POWER and GROUND signals delivered to the circuit within the lines 70. In addition, the **CLOCK signal** is delivered to the clock generator 16 and the decoder circuit 18 from the C.sub.O pin. The FUNCTION signal is. . .

DETD It should be noted that the **CLOCK signal** delivered to the clock generator 16 and the decoder circuit 18 is a merged function signal in that it is. . . 40 is also a merged function signal in that it provides, by appropriate coding techniques and in conjunction with the **CLOCK signal**, mode selection, memory address, data input and data output functions.

DETD . . . element 40 for proper recirculation of the data, and to the other components within the memory device 10 requiring a **clock signal**.

CLM What is claimed is:

. . . a ground level signal, comprising: a memory element; at least two external terminals; and signal processing means for receiving a **first signal** applied to one of said external terminals and a second signal applied to the other of said external terminals, said. . .

2. The memory device of claim 1, wherein **first signal** includes substantially periodic clock pulses and wherein said signal processing means comprises rectification means including a counter circuit for counting. . .

. . . at least two external pins and requiring a power signal and a ground level signal: rectification means for receiving a **first signal** applied to one of said external pins and a second signal applied to the other of said external pins, said. . .

5. The memory device of claim 4, wherein said **first signal** includes substantially periodic clock pulses and wherein said rectification means includes a capacitor, switch means and a counter circuit for. . .

. . . In a memory device having an internal power supply for receiving a power signal and a ground level signal; a **first pin** for receiving a first, substantially periodic signal; a second pin for receiving a second signal; and rectification circuit means connected.

. . . device claim 6, wherein said rectification means includes a counter circuit for counting the number of cycles in said **first signal**, and for generating an enabling signal after a predetermined number of cycles are counted.

. . . 7, wherein said rectification means further includes switching means for receiving said enabling signal and in response thereto connecting said **first pin** to a first, power input terminal of the internal power supply, and said second pin to a second, ground input. . .

. . . said first and second internal terminals for a period after said predetermined number of cycles are counted in which said **first signal** is positive.

13. In a memory device in the form of an integrated circuit structure: a

first pin for receiving a first synchronizing signal; means for detecting a change in said first synchronizing signal for enabling said memory device; a **second pin** for receiving a **second signal**, including memory address, data input, and internally-generated data output component signals; means for mode selecting said memory device in response. . . an internal power supply for receiving a power signal and a ground level signal; and rectification means for receiving the **first signal** and the **second signal** on said first and second external pins and in response thereto providing said power signal and said ground level signal. . .

. . . wherein said rectification means includes switching means and a counter circuit, said counter circuit for counting the pulses in said **first signal** and after a predetermined number of said pulses are counted, providing an enabling signal to said switching means for operatively. . .

15. A method for eliminating the external power and ground terminals on a memory device, comprising: providing a **first signal** on a first external pin having periodic pulses; providing a second signal on a second external pin which periodically is. . .

. . . number of pulses received at said first external pin and after a predetermined number of pulses are received at said **first pin**, generating an enabling signal for causing said first external pin and said second external pin to be connected to the. . .

=> d l27 kwic

L27 ANSWER 1 OF 1 USPATFULL

SUMM . . . applying power to the microcontroller device. In other words, the situation here involved a microcontroller that would not have a **reset signal**, either from an external **reset signal** input to the device via a **reset pin** or via some type of on chip software-generated **reset signal** well known to those skilled in the art. Since no **reset signal** was available for the microcontroller here involved, once V.sub.DD was applied to the device, there was no way to stop. . . the device. Thus, for the purpose of discussion here, the term "free-running microcontroller" means a microcontroller without an externally provided **reset signal**, and without any type of on chip software or hardware induced **reset signal** for the microcontroller, or at least if such a software or hardware induced **reset signal** could be established, it has not been so established. In other words, a free-running microcontroller (which is the area of concern for the

instant inv[redacted]tion) has no **reset signal** to st[redacted] it
from runni[redacted]nce V.sub.DD has been applied [redacted] the microcontroller.
DETD . . . referred to as "SMED or SMEDL"). Note that the term "free-running microcontroller" means a microcontroller 10 without an externally provided **reset signal** to a **reset pin**, and without any type of on chip, software or hardware induced **reset signal** for the microcontroller 10, or at least if such a software or hardware induced **reset signal** could be established, it has not been so established. In other words, free-running microcontroller 10 has no **reset signal** to stop it from running once V.sub.DD has been applied. Also, note that the three vertical dots shown between the. . .
DETD . . . a reset pin, the device, as configured, would not be free-running, but rather normal operation could be interrupted by the **test mode**. In this case, the device 10 would still include SMEDL 18 operating as previously discussed, and the claimed methodology of. . . first applying the test voltage followed by V.sub.DD could apply to the case of either a free-running or a non-free-running **microcontroller device**. Additionally, FIG. **1** shows each pin 12 as an I/O pin; however, those skilled in the art realize that the inventive structure and. .

types of pins well known to those skilled in the art could be implemented to the device 10 of FIG. **1**. In that case, those skilled in the art would recognize that such trivial changes would not significantly depart from the. . .

=> d l26 kwic 1-2

L26 ANSWER 1 OF 2 USPATFULL
DETD . . . a reset pin, the device, as configured, would not be free-running, but rather normal operation could be interrupted by the **test mode**. In this case, the device 10 would still include SMEDL 18 operating as previously discussed, and the claimed methodology of. . . first applying the test voltage followed by V.sub.DD could apply to the case of either a free-running or a non-free-running **microcontroller device**. Additionally, FIG. **1** shows each pin 12 as an I/O pin; however, those skilled in the art realize that the inventive structure and. .

types of pins well known to those skilled in the art could be implemented to the device 10 of FIG. **1**. In that case, those skilled in the art would recognize that such trivial changes would not significantly depart from the. . .

L26 ANSWER 2 OF 2 USPATFULL
DETD . . . 21 or pulled down to Vss by transistor 22. Typically, inverter 20 is used to provide an output from the **microcontroller device**. The **test mode** signal, as well as address lines, described earlier in reference to FIGS. **1** and 2, are each coupled from the **microcontroller device** through such inverters as shown in FIG. 3 as V.sub.IN.

=> d l21 kwic

L21 ANSWER 1 OF 1 USPATFULL
CLM What is claimed is:
. . . as set forth in claim 10, wherein said means for placing comprises: a
power-on reset circuit for generating a power-on **reset signal**; a NOR gate for asserting a network status signal in

response to said power-on reset circuit; and a NAND gate for asserting a tri-state signal in response to said power-on **reset signal** and said NOR gate.

. . . communications interface circuit as set forth in claim 21, wherein said means for placing comprises: means for generating a power-on **reset signal**; means for asserting a network signal in response to said means for detecting; and AND means for asserting a tri-state. . .

. . . The method as set forth in claim 27, wherein said detecting step further comprises the steps of: determining if said **second pin** is within said predetermined voltage range generally concurrent in time to detecting if said **first pin** is within the predetermined voltage range; asserting a **second signal** in response to determining that said **second pin** is within said predetermined voltage range; and asserting a third signal in response to said **first signal** and said **second signal**.

32. The method as set forth in claim 31, wherein said placing step comprises the steps of: generating a power-on **reset signal**; asserting a network signal in response to said generating step; and asserting a tri-state signal in response to said generating. . .

. . . as set forth in claim 42, wherein said means for placing comprises: a power-on reset circuit to generate a power-on **reset signal**; a NOR gate to assert a network signal in response to said means for detecting; and NAND means for asserting a tri-state signal in response to said power-on **reset signal** and said NOR gate.

=> d l20 kwic 1-2

L20 ANSWER 1 OF 2 USPATFULL

SUMM . . . damaged. The DAB preferably includes a keepalive clocking circuit that connects to the clock pins of the HME to provide **clock signals** to the HME circuitry. The keepalive circuitry keeps the HME refreshed when it is not being accessed by the HMS.

DETD TABLE 1

Signals	Direction	Description
CLK10MHZ	From PEL	The two keep-alive
CLK1MHZ	to DAB	**clock signals**.
EECLK	From PEL	The clock to the DAB
	to DAB	EEPROM
EEIN	From PEL	The serial input to
	to DAB	the DAB. . .

DETD . . . shows keepalive clock circuitry 154 of FIG. 1. Referring to FIGS. 1 and 22, system connector 102 receives two keepalive **clock signals** and an enable signal from the PEL. The system connector provides these signals to the keepalive clock circuitry via parallel. . .

CLM What is claimed is:

. . . modeling system is powered including: i. electrostatic charge dissipation circuitry to dissipate electrostatic charge; ii. a first segment including a **first pin** of a first length coupled to the electrostatic charge dissipation circuitry; iii. ground

equalization circuitry to equalize ground levels of the connector, the hardware modeling system and the hardware modeling element; iv. a second segment including a **second pin** of a second length coupled to the ground equalization circuitry; v. power supply control circuitry to supply power from the. . . length is longer than the third length such that when the connector is inserted into the hardware modeling system, the **first pin** engages the hardware modeling system first, the **second pin** engages the hardware modeling system second and the third pin engages the hardware modeling system third; b. a grid adapter. . . and providing electrical signals to the hardware modeling element including a voltage regulator coupled to the connector for receiving a **first signal** and forming a **second signal**, and a switch for selecting between a selective one of the **first signal** and the **second signal** for powering the hardware modeling element; and d. a memory circuit for storing and providing information to the hardware modeling. . .

L20 ANSWER 2 OF 2 USPATFULL

DETD . . . lines 70 to provide the POWER and GROUND signals delivered to the circuit within the lines 70. In addition, the **CLOCK signal** is delivered to the clock generator 16 and the decoder circuit 18 from the C.sub.O pin. The FUNCTION signal is. . .

DETD It should be noted that the **CLOCK signal** delivered to the clock generator 16 and the decoder circuit 18 is a merged function signal in that it is. . . 40 is also a merged function signal in that it provides, by appropriate coding techniques and in conjunction with the **CLOCK signal**, mode selection, memory address, data input and data output functions.

DETD . . . element 40 for proper recirculation of the data, and to the other components within the memory device 10 requiring a **clock signal**.

CLM What is claimed is:

13. In a memory device in the form of an integrated circuit structure: a **first pin** for receiving a first synchronizing signal; means for detecting a change in said first synchronizing signal for enabling said memory device; a **second pin** for receiving a **second signal**, including memory address, data input, and internally-generated data output component signals; means for mode selecting said memory device in response. . . an internal power supply for receiving a power signal and a ground level signal; and rectification means for receiving the **first signal** and the **second signal** on said first and second external pins and in response thereto providing said power signal and said ground level signal. . .

=> d l10 kwic 1-15

L10 ANSWER 1 OF 15 USPATFULL

CLM What is claimed is:

. . . modeling system is powered including: i. electrostatic charge dissipation circuitry to dissipate electrostatic charge; ii. a first segment including a **first pin** of a first length coupled to the electrostatic charge dissipation circuitry; iii. ground equalization circuitry to equalize ground levels of the connector, the hardware modeling system and the hardware modeling element; iv. a second segment including a **second pin** of a second length coupled to the ground equalization circuitry; v. power supply control circuitry to supply power from the. . . length is longer than the third length such that when the connector is inserted into the hardware

modeling system, the **first pin** engages the hardware modeling system first, the **second pin** engages the hardware modeling system second and the third pin engages the hardware modeling system third; b. a grid adapter. . . . and providing electrical signals to the hardware modeling element including a voltage regulator coupled to the connector for receiving a **first signal** and forming a **second signal**, and a switch for selecting between a selective one of the **first signal** and the **second signal** for powering the hardware modeling element; and d. a memory circuit for storing and providing information to the hardware modeling. . .

L10 ANSWER 2 OF 15 USPATFULL
CLM What is claimed is:
. . . test pattern signal and a driver enable signal; a first driver for directly supplying a first drive signal to a **first pin** of the DUT through a **first signal** path, the first drive signal being produced by a first combination of the drive voltages and the test pattern signal; a second driver for directly supplying a second drive signal to a **second pin** of the DUT through a **second signal** path, the second drive signal being produced by a second combination of the drive voltages and the test pattern signal;. . . and a comparator, a first input of which is connected to both an output of the second driver and the **second signal** path, and a second input of which is provided with a reference voltage, for comparing an output signal of the DUT from the **second signal** path with the reference voltage; wherein the first driver is disabled and the second driver is enabled by the driver. . .
. . . driver for directly supplying a first drive signal formed by the drive voltages and the test pattern signal to a **first pin** of the DUT through a **first signal** path; a second driver for directly supplying a second drive signal formed by the drive voltages and the test pattern signal to a **second pin** of the DUT through a **second signal** path; a control circuit connected between the first and second drivers and the wave formatter for controlling the operation of. . . and a comparator, a first input of which is connected to both an output of the second driver and the **second signal** path, and a second input of which is provided with a reference voltage, for comparing an output signal of the DUT from the **second signal** path with the reference voltage; wherein the control circuit disables the first driver so that the output of the first. . .

L10 ANSWER 3 OF 15 USPATFULL
AB . . . to the signal input terminal of the bus driver circuit and they have separate respective outputs connected to first and **second pins** respectively of the second part of the input connector. A **first signal** distribution bus on the signal distribution board extends from a **first pin** of the first part of the input connector in a first direction and a **second signal** distribution bus on the signal distribution board extends from a **second pin** of the first part of the input connector in a second direction, opposite the first direction. The first and **second pins** of the first part of the input connector are connected to the first and **second pins** respectively of the second part of the input connector when the first and second parts of the input connector are. . .

SUMM . . . drivers each having an input connected to said signal input terminal and having separate respective outputs connected to first and **second pins** respectively of the second part of the input connector, a **first signal** distribution bus on the signal distribution board extending from a **first pin** of the first part of the input connector in said first direction and connected to pins of the first parts of the first set of distribution connectors, a **second signal** distribution bus on the signal distribution board extending from a **second pin** of the first part of the input connector in said second direction and connected to pins of the first parts of the second set of distribution connectors, and wherein the first and **second pins** of the first part of the input connector are connected to the first and **second pins** respectively of the second part of the input connector when the first and second parts of the input connector are. . .

SUMM . . . drivers each having an input connected to said signal input terminal and having separate respective outputs connected to first and **second pins** respectively of the second part of the input connector, a **first signal** distribution bus on the signal distribution board extending from a **first pin** of the first part of the input connector in a first direction, and a **second signal** distribution bus on the signal distribution board extending from a **second pin** of the first part of the input connector in a second direction, opposite said first direction, and wherein the first and **second pins** of the first part of the input connector are connected to the first and **second pins** respectively of the second part of the input connector when the first and second parts of the input connector are. . .

CLM What is claimed is:

. . . drivers each having an input connected to said signal input terminal and having separate respective outputs connected to first and **second pins** respectively of the second part of the input connector, a **first signal** distribution bus on the signal distribution board extending from a **first pin** of the first part of the input connector in said first direction and connected to pins of the first parts of the first set of distribution connectors, a **second signal** distribution bus on the signal distribution board extending from a **second pin** of the first part of the input connector in said second direction and connected to pins of the first parts of the second set of distribution connectors, and wherein the first and **second pins** of the first part of the input connector are connected to the first and **second pins** respectively of the second part of the input connector when the first and second parts of the input connector are. . .

8. An interconnection arrangement according to claim 7, further comprising a **first signal** distribution bus on the signal distribution board extending from a **first pin** of the first part of the first input connector in said first direction and connected to pins of the first parts of the first set of distribution connectors, a **second signal** distribution bus on the signal distribution board extending from a **second pin** of the first part of the first input connector in said second direction and connected to pins of the first. . . of the second set of distribution connectors, a third signal distribution bus on the signal distribution board extending from a **first pin** of the first part of the second input connector in said first direction and connected to pins of the first.

. the first set of distribution connectors, and a fourth signal distribution bus on the signal distribution board extending from a **second pin** of the first part of the second input connector in said second direction and connected to pins of the first.

. . . drivers [redacted]h having an input connected to [redacted]id signal input terminal and having separate respective outputs connected to first and **second pins** respectively of the second part of the input connector, a **first signal** distribution bus on the signal distribution board extending from a **first pin** of the first part of the input connector in a first direction, and a **second signal** distribution bus on the signal distribution board extending from a **second pin** of the first part of the input connector in a second direction, opposite said first direction, and wherein the first and **second pins** of the first part of the input connector are connected to the first and **second pins** respectively of the second part of the input connector when the first and second parts of the input connector are. . .

L10 ANSWER 4 OF 15 USPATFULL

CLM What is claimed is:

1. An interface device on a printed circuit board comprising: a plurality of **first pins** for connecting to a first external device supporting a first interface standard; a plurality of **second pins** for connecting to a second external device supporting a second interface standard; a **first signal** line connected to a first one of said **first pins** and to a first one of said **second pins**; a **second signal** line connected to a second one of said **first pins** and to a second one of said **second pins** ; a third signal line connected to a third one of said **first pins** and to a third one of said **second pins**; and a driver/receiver circuit having a first input connected to said **first signal** line for receiving respective signals in accordance with said first and second interface standards and an output connected to said **second signal** line for outputting respective signals in accordance with said first and second interface standards, said driver/receiver circuit having a second. . .

2. An interface device on a printed circuit board comprising: a plurality of **first pins** for connecting to a first external device supporting a first interface standard; a plurality of **second pins** for connecting to a second external device supporting a second interface standard; a **first signal** line connected to a first one of said **first pins** and to a first one of said **second pins**; a **second signal** line connected to a second one of said **first pins** and to a second one of said **second pins** ; a third signal line connected to a third one of said **first pins** and to a third one of said **second pins**; and a driver/receiver circuit having an input connected to said **first signal** line for receiving respective signals in accordance with said first and second interface standards and a first output connected to said **second signal** line for outputting respective signals in accordance with said first and second interface standards, said driver/receiver circuit having a second. .

3. An interface device on a printed circuit board comprising: a plurality of **first pins** for connecting to a first external device supporting a first interface standard; a plurality of **second pins** for connecting to a second external device supporting a second interface standard; a **first signal** line connected to a first one of said **first pins** and to a first one of said **second pins**; a **second signal** line connected to a second one of said **first pins** and to a second one of said **second pins** ; a third signal line connected to a third one of said **first pins** and to a third one of said **second pins**; a fourth signal line connected to a fourth one of said **first**

pins and to a fourth one of said **second pins** ; a first driver/receiver circuit having an input connected to said **first signal** line for receiving respective signals in accordance with said first and second interface standards and an output connected to said **second signal** line for outputting respective signals in accordance with said first and second interface standards; and a second driver/receiver circuit having. . .

L10 ANSWER 5 OF 15 USPATFULL
CLM What is claimed is:
. . . The method as set forth in claim 27, wherein said detecting step further comprises the steps of: determining if said **second pin** is within said predetermined voltage range generally concurrent in time to detecting if said **first pin** is within the predetermined voltage range; asserting a **second signal** in response to determining that said **second pin** is within said predetermined voltage range; and asserting a third signal in response to said **first signal** and said **second signal**.

L10 ANSWER 6 OF 15 USPATFULL
AB . . . and the second input, wherein the comparator has an output that

produces an output signal in response to receiving a **first signal** from the second input and a **second signal** from the memory array; a first transistor having a gate connected to the output of the comparator, a first source/drain connected to a **first pin**, and a second source/drain connected to a **second pin**; and a second transistor having a gate connected to the output of the comparator, a first source/drain connected to the. . .
SUMM . . . and the second input, wherein the comparator has an output that

produces an output signal in response to receiving a **first signal** from the second input and a **second signal** from the memory array; a first transistor having a gate connected to the output of the comparator, a first source/drain connected to a **first pin**, and a second source/drain connected to a **second pin**; and a second transistor having a gate connected to the output of the comparator, a first source/drain connected to the. . .
CLM What is claimed is:
. . . RAM comprising: a first input for receiving a first portion of an address; a second input for receiving data; a **first pin**; a **second pin**; an output pin; a memory array connected to the first and second inputs; a comparator connected to the memory array. . . and the second input, wherein the comparator

has an output that produces an output signal in response to receiving a **first signal** from the second input and a **second signal** from the memory array; a first transistor having a gate connected to the comparator output, a first source/drain connected to the **first pin**, and a second source/drain connected to the **second pin**; and a second transistor having a gate connected to the comparator output, a first source/drain connected to the output pin,. . .
. . . bus; plurality of tag RAMs including at least a first and a last tag RAM, each tag RAM having: a **first pin**; a **second pin**; an output pin; a memory array connected to the first input; a comparator connected to the memory array and the second input, wherein the comparator has an output that produces an output signal in response to receiving a **first signal** from the second input and a **second signal** from the memory array; a first transistor having a gate connected to the output

of the comparator, a first source/drain connected to the **first pin**, and a second source/drain connected to the **second pin**; and a second transistor having a gate connected to the output of the comparator, a first source/drain connected to the output pin, and a second source/drain connected to a lower power supply voltage source; and the **first pin** of the first tag RAM being connected an upper power supply voltage; the **second pin** of each tag RAM, other than the last tag RAM, being connected to the **first pin** of a subsequent tag RAM; the output pin of each tag RAM being connected to the match bus; and the **second pin** of the last tag RAM being connected to the match bus, wherein a NOR function is provided between output pins. . .

L10 ANSWER 7 OF 15 USPATFULL
CLM What is claimed is:
. . . to monitor communications exchanged between said first end user and said second end user, said connect means further comprising a **first pin** connector for coupling signals out of said digital communications link, a **second pin** connector for coupling signals into said PC, a **first signal** conducting path coupling pin numbers 1, 2 and 7 of said **first pin** connector to pin numbers 1, 3 and 7 respectively of said **second pin** connector, a **first signal** shorting path coupled to pin numbers 4 and 5 of said **second pin** connector and a **second signal** shorting path coupled to pin numbers 6, 8 and 20 of said **second pin** connector, a third pin connector for coupling signals into said digital communication link, a fourth pin connector for coupling signals out of said PC, a **second signal** conducting path coupling pin numbers 1, 3 and 7 of said third pin connector to pin numbers 1, 3 and. . .

L10 ANSWER 8 OF 15 USPATFULL
CLM What is claimed is:
10. The module of claim 7 wherein said transmit and receive switch comprises means forming a **first signal** pathway from said first coaxial connection to said high-power amplifier, with a **first PIN** diode connected in shunt with the **first signal** pathway at a point equal to one-quarter wavelength of the electromagnetic energy being transmitted and received, means forming a **second signal** pathway from said first coaxial connection to said low-noise amplifier with a **second PIN** diode connected in shunt with the **second signal** pathway at a point equal to one-quarter wavelength of the electromagnetic energy being transmitted and received, and first and second dc connections to said first and **second PIN** diodes, respectively, to control the impedance of the first and **second signal** pathways at the first coaxial connection.

L10 ANSWER 9 OF 15 USPATFULL
DETD . . . introduced into the recording and/or reproducing apparatus with the upper surface of the disk cartridge 1 directed upwards and the **first signal** recording surface of the disk 6 facing the optical pickup unit 44, the **first pin** 57 on the distal end of the arm 51 is positioned facing to the opening 29 of the shutter member. . . introduced into the recording and/or reproducing apparatus with the lower surface of the disk cartridge 1 directed

upwards and [redacted] **second signal** recording surface of the disk 6 [redacted]ng the optical pickup unit, th[redacted]**econd pin** 58 implanted on the distal end of the arm 52 is positioned facing to the opening 29 of the shutter. . .

L10 ANSWER 10 OF 15 USPATFULL
CLM What is claimed is:
. . . circuit for attenuating an RF signal in response to a voltage level of a control signal, the circuit comprising: a **first PIN** diode having an anode and a cathode, a first one of the anode and cathode of said **first PIN** diode being adapted to transport the RF signal; a **second PIN** diode having an anode and a cathode, a first one of the anode and cathode of said **second PIN** diode being adapted to receive a common potential, and a second one of the anode and cathode of said **second PIN** diode being coupled to a second one of the anode and cathode of said **first PIN** diode; a first differential amplifier having first and **second signal** inputs and an output, the **first signal** input of said first amplifier being adapted to receive a first reference potential, the **second signal** input of said first amplifier being adapted to receive the control signal, and the output of said first amplifier being coupled to one of the anode and cathode of said **first PIN** diode; a second differential amplifier having first and **second signal** inputs and an output, the **first signal** input of said second amplifier being adapted to receive a second reference potential, the **second signal** input of said second amplifier being adapted to receive the control signal, and the output of said second amplifier being coupled to the second one of the anode and cathode of said **second PIN** diode; means, coupled to said first differential amplifier, for setting a gain parameter of said first differential amplifier at a. . .

L10 ANSWER 11 OF 15 USPATFULL
CLM What is claimed is:
. . . means, a first electrical signal transmitter mounted on the jaw means for engaging the radial surface of the workpiece, and **first signal** transmission and evaluating means extending from the first transmitter to the exterior of the chuck body through the jaw means. . . first contact bar means, and first spring means urging said first contact pin means toward said first bar means, said **first pin** means and said first bar means being interengageable against the force of said first spring means when said piston is. . . jaw means for sensing the clamping force of the jaw means on the workpiece when the workpiece is clamped thereby, **second signal** transmission and evaluating means extending from the second transmitter to the exterior of the chuck body through the jaw means. . . second contact bar means, and second spring means urging said second contact pin means toward said second bar means, said **second pin** means and said second bar means also being interengageable against the force of said second spring means when said piston. . .

L10 ANSWER 12 OF 15 USPATFULL
CLM What is claimed is:
13. In a memory device in the form of an integrated circuit structure: a **first pin** for receiving a first synchronizing signal;

means for de[redacted]ting a change in said first sy[redacted]hronizing signal for enabling sa[redacted]emory device; a **second pin** fo[redacted] receiving a **second signal**, including memory address, data input, and internally-generated data output component signals; means for mode selecting said memory device in response. . . an internal power supply for receiving a power signal and a ground level signal; and rectification means for receiving the **first signal** and the **second signal** on said first and second external pins and in response thereto providing said power signal and said ground level signal. . .

L10 ANSWER 13 OF 15 USPATFULL

CLM What is claimed is:

10. In a memory device in the form of an integrated circuit structure: a **first pin** for receiving a first synchronizing signal; means for detecting a change in said first synchronizing signal for enabling said memory device; a **second pin** for receiving a **second signal**, including memory address, data input, and internally-generated data output component signals; means for mode selecting said memory device in response. . . an internal power supply for receiving a power signal and a ground level signal; and rectification means for receiving the **first signal** and the **second signal** on said first and second external pins and in response thereto providing said power signal and said ground level signal. . . means, said threshold detector means for providing an enabling signal when a predetermined difference in voltage between said first and **second signals** is sensed, said switching means for receiving said enabling signal and in response thereto for operatively connecting said first and. . .

L10 ANSWER 14 OF 15 USPATFULL

AB . . . and second electrical signals at predetermined time intervals, includes a servo unit for receiving the electrical signals. Upon receiving the **first signal**, the servo unit drives a first lever to contact and drive a **first pin** to a first position, and upon receiving the **second signal**, the servo unit drives a second lever to contact and drive a **second pin** to a second position. A first clutch is fixed to the **first pin** and is adapted to uncouple the minute and hour hand works from the mainspring assembly when the **first pin** is driven to the first position and to drive the minute and hour hand works to a first time setting. A second clutch is fixed to the **second pin** and is adapted to drive the minute and hour hand works to a second time setting when the **second pin** is driven to the second position and thereupon to couple the minute and hour hand works to the mainspring assembly.

SUMM . . . first and second electrical signals at pre-determined intervals, includes a servo unit for receiving the electrical signals. Upon receiving the **first signal**, the servo unit drives a first lever to contact and drive a **first pin** to a first position. Upon receiving the **second signal**, the servo unit drives a second lever to contact and drive a **second pin** to a second position. A first clutch is fixed to the **first pin** and is adapted to uncouple the minute and hour hand works from a mainspring assembly when the **first pin** is driven to the first position and to drive the minute and hour hand works to a first time setting. A second clutch is fixed to the **second pin** and is adapted to drive the minute and hour hand works to a second time setting when the **second pin** is driven to the second position and thereupon to couple the minute and hour hand works to the mainspring assembly.

CLM What is claimed is:
. . . electrical signals at predetermined time intervals, comprising: (a) a
servo unit for receiving the electrical signals, and upon receiving the **first signal**, the servo unit driving a first lever to contact and drive a **first pin** to a first position, and upon receiving a **second signal**, the servo unit driving a second lever to contact and drive a **second pin** to a second position; (b) a first clutch fixed to the **first pin**, rotatively coupled to a main drive shaft of a main drive assembly, and drivably connected to minute and hour hand. . . works, the first clutch adapted to uncouple the minute and hour hand works from the main drive assembly when the **first pin** is driven to the first position, the first clutch further adapted to drive the minute and hour hand works to a first time setting;
and (c) a second clutch fixed to the **second pin**, rotatively coupled to the main drive shaft of the main drive assembly, and drivably connected to the minute and hour. . . works, the second clutch adapted to drive the minute and hour hand works to a second time setting when the **second pin** is driven to the second position and thereupon to couple the minute and hour hand works to the main drive. . .
. . . (b) a servo unit for receiving the electrical signals converted by the receiving and converting means, and upon receiving the **first signal**, the servo unit driving, in a clockwise direction, a biased first lever through a predetermined arc thereby contacting and driving a **first pin** to a first position, and upon receiving a **second signal**, the servo unit driving, in a counterclockwise direction, a biased second lever through a predetermined arc thereby contacting and driving a **second pin** to a second position; (c) a first clutch fixed to the **first pin**, rotatively coupled to a main drive shaft of a main drive assembly, and drivably connected through a gear arrangement
to. . . works, the first clutch adapted to uncouple the minute and hour hand works from the main drive assembly when the **first pin** is driven to the first position, the first clutch further adapted to drive the minute and hour hand works in a clockwise direction
to a first time setting; and (d) a second clutch fixed to the **second pin**, rotatively coupled to the main drive shaft of the main drive assembly, and drivably connected through the gear arrangement to. . . adapted to drive the minute and hour hand works in a counterclockwise direction to a second time setting when the **second pin** is driven to the second position and thereupon to couple the minute and hour hand works to the main drive.
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L10 ANSWER 15 OF 15 USPATFULL
CLM What is claimed is:
. . . reverberation conditions comprising: means for detecting the envelope
of return acoustic energy during each ping period; means for storing a **first signal** representative of the amplitude of the detected envelope at a first predetermined time during a **first ping** period and for storing a **second signal** representative of the amplitude of the detected envelope at a second predetermined time during the **first ping** period subsequent to the first time, the first and second stored signals representing an expected reverberation condition for ping periods subsequent to the **first ping** period; and, means for controlling the gain of the sonar receiving circuit during a **second ping** period subsequent to the **first**

ping period in response both to the amplitude of the detected envelope in the **second ping** period and to the first and second stored signals.

. . . to minimize the effects of changing reverberation conditions comprising the steps of: detecting the envelope of return energy during a **first ping** period; storing a **first signal** representative of the amplitude of the detected envelope at a first time during the **first ping** period; storing a **second signal** representative of the amplitude of the detected envelope at a second time during the **first ping** period, the first and second stored signals representing an expected reverberation condition for ping periods subsequent to the **first ping** period; detecting the envelope of return energy during a **second ping** period subsequent to the **first ping** period; and, controlling the gain of the receiving circuit in response to the amplitude of the detected envelope in the **second ping** period and to the first and second stored signals.